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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,568	01/22/2002	Mou-Shiung Lin	JCLA8533	6093

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/13/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/055,568	LIN ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *219-223,228-236,238-242,250-257,259,260 and 262-267* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *219-223,228-236,238-242,250-257,259,260 and 262-267* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the request for continued examination filed December 11, 2006.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 220, 263 and 267 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. There is no antecedent basis for "said first patterned circuit layer" in claims 220 and 263 or a "said first patterned circuit layer" in claim 263. Applicant deleted the antecedent in his amendment.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 219- 223, 228-236, 250, 251, 257, 259, 260, 263, 264, 266 and 267 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama[1] (U.S.2001/0042901) in combination with in combination with Ahn (U.S. 2003/0020180).

7. Maruyama (Fig. 2, 10, 17A-D, 19) discloses:

(cl. 219, 264) a chip package comprising: a preformed[2] substrate (11) comprising silicon, semiconductor material (Par.0083), said substrate having no circuitry; only one die (12; Fig. 19) joined with said substrate (Fig. 2); and a patterned line (e.g. 15) over said only one die and over said substrate; a first insulating layer (20) comprising a first portion over said only one preformed die (e.g. directly above chip circuit; Fig. 19) and a second portion over preformed substrate but not over said die (e.g. insulation to left and right of die);

---

[1] Note that Saia (U.S. 5,874,770) could be used to evidence non-obviousness. The prior art discloses the claimed invention including passive components in its redistribution layer on a support substrate that may be various materials. As such, the selection of silicon would have been prima facie obvious. See paragraph 9 of this office action.

[2] With respect to preformed limitation, this is a process limitation that does not impart a structural difference than that shown by chips embedded in a wafer. Note, "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

(cl. 263) wherein said die comprising a thin- film circuit layer/ multiple active devices formed therein (e.g. within die; Fig. 10), having patterned line having a thickness greater than that of said thin-film circuit layer (e.g. can see 15);

(cl. 223) wherein said patterned line connects multiple portions of said only one die (e.g. IC within die send signal though 15);

(cl. 224) an insulating layer (20) between said only one die and said patterned line;

(cl. 227, 231) said insulating layer comprises a porous (e.g. all material has a level of porosity) chip package;

(cl. 228, 232, 235) further comprising an insulating layer (22) over said patterned line;

(cl. 236, 237, 243, 244) further comprising passive device comprising a capacitor[3] over said substrate;

(cont. cl. 243, 251, 266) said only one preformed die having a top surface and a lower surface said substrate being under said lower surface of said only one preformed die, said top surface of said only one preformed die being at a horizontal level (e.g. top pf chip and top of substrate co-planar) wherein said passive device is over said horizontal level ("passive elements...on a redistribution layer"; Fig. 17C);

(cl. 250) wherein an opening (e.g. space taken by 12) is in said substrate and accommodates said only one die (Fig. 19);

(cl. 257) with the insulation (e.g. 22) over (e.g. above) said substrate and around said only die (e.g. to left and right of die);

(cl. 260) further comprising a bump (16) on line;

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[3] Characteristic of wiring separated by insulation.

(cl. 266) wherein an opening (e.g. space taken by 16, 21) is in said first and second layer and connection through opening;

(cl. 267) and a portion of line not under die (e.g. farthest left portion of 15; Fig. 17C).

8. Murayama discloses the same invention as claimed except that its insulation is disclosed as SiO instead of BCB or polyimide, Ahn (Par. 0036) shows that SIO, BCB and polyimide produce equivalent structures known in the art. Therefore, because these two insulators are art recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to select either material for the other, e.g. polyimide for BCB insulator or SiO.

9. Moreover, applicant has not disclosed that his selection of material (e.g. gold, copper, BCB, Polyimide; see footnote 6) produces unexpected results or otherwise critical. As such, the selection of the claimed material for example BCB or polyimide as an insulator or gold and copper for wirings would have been obvious to one of ordinary skill in the art, since it has been held that selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination. Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945); See M.P.E.P 23144.07.

10. With respect to the intended use limitations of claim 221 and 222 that for example the lines are power or ground bus, the prior art forms the same structure as the claimed invention. As such, the claim would not be distinguishable over the prior art, since it has been held that the manner in which a claimed apparatus is intended to be

employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

11. Claim 262 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (U.S.2001/0042901) as applied to claim 219 and further in combination with in combination with Alcoe et al. (U.S. 2002/0135063).

12. Murayama further discloses a terminal (14, 16), but does not appear to disclose its being gold.

13. However, Alcoe (Par. 0010) discloses gold terminals/bumps.

14. It would have been obvious to one of ordinary skill in the art to form the terminal of gold as taught by Alcoe in order to provide electrically conductive terminal as required by Murayama (14,16). Furthermore, with the selection of material see paragraph 9 of this office action.

15. Claim 265 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (U.S.2001/0042901) as applied to claim 219 and further in combination with in combination with McIntrye (U.S. 6,555,469).

16. Murayama further discloses its wiring is a conductive layer (Par. 0086), but does not appear to disclose its layer being copper.

17. However, McIntrye (Col. 6, Lines 13-15) discloses copper for wiring/traces.

18. It would have been obvious to one of ordinary skill in the art to form the wiring of Murayama of copper as taught by McIntrye in order to provide electrically conductive

material as required by Murayama (Par. 0086). Furthermore, with the selection of material see paragraph 9 of this office action.

19. Claim 219- 223, 228-236, 238, 239, 250, 251, 257, 259, 260, 263-267 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. 6,867,499) and Ahn (U.S. 2003/0020180).

20. Tabrizi (Fig. 2, 5) discloses:

(cl. 219, 264) a chip package comprising: a preformed[4] (understood to be made separate from the chip/substrate) substrate (510) comprising silicon, semiconductor material (CLM 12 of Tabrizi), said preformed substrate having no circuitry (Fig. 5); only one preformed die (520) joined (e.g. 530) with said preformed substrate; and a patterned line (e.g. 560) over said only one preformed die and over said preformed substrate;

(cl. 220) wherein said preformed die comprising a thin- film circuit layer formed therein (e.g. within die; Col. 2, Lines 51-54), said patterned line having a thickness greater than that of said thin-film circuit layer (e.g. can see 560);

(cl. 223) wherein said patterned line connects multiple portions of said only one preformed die (e.g. IC within die send signal though 560);

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[4] Although the prior art discloses a preformed substrate and die, the limitation is a process limitation that does not impart a structural difference than for example and chip mounted to/on a substrate whether preformed or if the chip is made embedded in the substrate. Note, "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

an insulating layer (550) between said only one preformed die and said patterned line;

(cl. 226) said insulating layer comprises benzocyclobutene (BCB) (Col. 2, Lines 21-23 &39-40);

(cl. 231) said insulating layer comprises a porous (e.g. all material has a level of porosity) chip package;

(cl. 228, 232, 235) further comprising an insulating layer (570) over said patterned line;

(cl. 236, 238, 239) further comprising passive device comprising a capacitor/ inductor/ resistor over said substrate (Col. 5, Lines 1-4);

(cl. 250) wherein an opening (515) is in said preformed substrate and accommodates said only one preformed die (Fig. 5);

(cl. 251) said only one preformed die having a top surface and a lower surface said preformed substrate being under said lower surface of said only one preformed die, said top surface of said only one preformed die being at a horizontal level (e.g. top pf chip and top of substrate co-planar) wherein said passive device is over said horizontal level ("passive elements...on a redistribution layer"[5]; Col. 5, Lines 1-4);

(cl. 257) with the insulation (e.g. 570) over (e.g. above) said substrate and around said only die (e.g. to left and right of die);

(cl. 259) wherein insulation above pattern is an epoxy (Par. 0104)

(cl. 260) further comprising a solder bump (580; CLM 13 of Tabrizi) on said patterned;

(cl. 263) die is an integrated circuit and therefore has multiple active devices;

(cl. 265) with the pattern comprises copper (CLM 3 of Tabrizi);

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[5] Items 550 & 560 above horizontal forms part of redistribution layer.

(cl. 266) wherein an opening (e.g. space taken by wire) is in said first layer and connection through opening;

(cl. 267) and a portion of line not under die (e.g. farthest left and right portion of wire not directly over die).

21. Tabrizi does not appear to disclose that its insulation may be a polyimide.

22. However Tabrizi discloses the same invention as claimed except that its insulation is disclosed as BCB instead of polyimide, Ahn (Par. 0036) shows that both BCB and polyimide produce equivalent structures known in the art. Therefore, because these two insulators are art recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to select polyimide for BCB insulator.

23. Moreover, applicant has not disclosed that his selection of material, see paragraph 9 of this office action.

24. With respect to the intended use limitations of claim 221 and 222 that for example the lines are power or ground bus, see paragraph 10 of this office action.

25. Claim 240 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. 6,867,499) and Ahn (U.S. 2003/0020180) as applied to claim 219 and further in combination with Tahara et al. (U.S. 2002/0017730).

26. Neither Tabrizi or Ahn appear to disclose incorporating a filter as a passive device.

27. Tahara utilizes a filter as a passive device (Par. 0069).

28. It would have been obvious to one of ordinary skill in the art to incorporate a wave guide into the structure of Tabrizi in order to provide a passive component as required by Tabrizi (Col. 5, Lines 1-4).

29. Claim 241 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. 6,867,499) and Ahn (U.S. 2003/0020180) as applied to claim 236 and 243 and further in combination with Shuy et al. (U.S. 2003/0118738)

30. Neither Tabrizi or Ahn appear to disclose a wave-guide as a passive device.

31. Shuy utilizes a wave-guide as a passive device (e.g. CLM 8 of Shuy).

32. It would have been obvious to one of ordinary skill in the art to incorporate a wave guide into the structure of Tabrizi in order to provide a passive component as required by Tabrizi (Col. 5, Lines 1-4).

33. Claims 242 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. 6,867,499) and Ahn (U.S. 2003/0020180) as applied to claim 236 and 243 and further in combination with Jun et al. (U.S. 2002/0084510)

34. Neither Tabrizi or Ahn appear to discloses a MEMS as a passive device.

35. Jun utilizes a MEMS as a passive device (Abstract).

36. It would have been obvious to one of ordinary skill in the art to incorporate a MEMS into the structure of Tabrizi in order to provide a passive component as required by Tabrizi (Col. 5, Lines 1-4).

37. Claims 252-256 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. 6,867,499) and Ahn (U.S. 2003/0020180) as applied to claim 219 and further in combination with Korman (U.S 5,959,357)

38. Neither Tabrizi or Ahn appear to discloses its substrate comprising second layer, said first layer being on said second layer, wherein said first layer is the silicon and said second layer is a metal copper.

39. Korman (Fig. 3) utilizes a substrate comprising a first layer on a copper, second metal layer (22).

40. It would have been obvious to one of ordinary skill in the art to modify the silicon substrate of Tabrizi such that a portion is formed on a second layer that is a metal copper in order to provide a heat spreader as taught by Korman (Col. 4, Lines 55-56).

41. Claim 262 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. 6,867,499) and Ahn (U.S. 2003/0020180) as applied to claim 219 and further in combination with in combination with Alcoe et al. (U.S. 2002/0135063).

42. Tabrizi discloses a terminal/bump (21), but does not appear to disclose its being gold.

43. However, Alcoe (Par. 0010) discloses gold terminals/bumps.

44. It would have been obvious to one of ordinary skill in the art to form the terminal of gold as taught by Tabrizi in order to provide electrically conductive terminal as

required by Murayama (14,16). Furthermore, with the selection of material see paragraph 9 of this office action.

Response to Arguments

45. Applicant's arguments filed December 11, 2006 have been fully considered but they are not persuasive. Applicant contends that the claimed invention is patentable over the prior art, because Maruyama allegedly does not disclose a die, but circuits within a wafer. Applicant contends that a die is typically separated from the wafer. Examiner concurs. However, structurally as claimed there is no difference between defined circuit regions/ dice in a wafer and a die that is on a cavity within a wafer or substrate. As indicated in the office action, it is immaterial whether the substrate is preformed or not, because a patentability is defined by its structure not its process. Because applicant has not identified a structural difference, see for example applicant's Figure 2C, which is the same structure as the prior art.

46. With respect to Tabrizi, applicant contends that the claimed invention is patentable, because allegedly Tabrizi does not show a second portion of its insulation not over the die. Examiner disagrees, because the insulation includes areas/ portions to the left and right of chip that are not directly over the chip/die.

47. As for applicant's traversal of Nagakari based on no motivation to form an insulation layer over the die, it is deemed moot because the feature of being over the die was not relied on. Rather the reference was used only to evidence the common use

of various types of materials, such as BCB and polyimide, to provide insulation. As such, the rejection is deemed proper.

Conclusion

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses examples of chips with a redistribution layer formed in a silicon substrate cavity; copper wiring, see e.g., Saia et al (U.S. 5,874,770).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D.
March 2, 2007

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